

**S/N Unknown**

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant:	Siva G. Narendra et al.	Examiner:	Unknown
Serial No.:	Unknown	Group Art Unit:	Unknown
Filed:	Herewith	Docket:	884.575US2
Title:	CURRENT REFERENCE APPARATUS AND SYSTEMS		
Assignee:	Intel Corporation		

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**INFORMATION DISCLOSURE STATEMENT**

MS Patent Application  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement.

Pursuant to 37 C.F.R. §1.98(d), copies of the listed documents are not provided as these references were previously cited by or submitted to the U.S. Patent Office in connection with Applicants' prior U.S. application, Serial No. 10/025047, filed on December 19, 2001, which is relied upon for an earlier filing date under 35 U.S.C. §120.

INFORMATION DISCLOSURE STATEMENT

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Assignee: Intel Corporation

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The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

SIVA G. NARENDRA ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

P.O. Box 2938

Minneapolis, MN 55402

(612) 349-9592

Date Oct. 20, 2003

By Ann M. McCrackin

Ann M. McCrackin

Reg. No. 42,858

"Express Mail" mailing label number: EV332571603US

Date of Deposit: October 20, 2003

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to The Commissioner for Patents, Mail Stop Patent Application, P.O. Box 1450, Alexandria, VA 22313-1450.

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number Unknown

Filing Date Even Date Herewith

First Named Inventor Narendra, Siva

Group Art Unit Unknown

Examiner Name Unknown

Sheet 1 of 1

Attorney Docket No: 884.575US2

**US PATENT DOCUMENTS**

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US-5,929,697	07/27/1999	Chang, Kok C.	327	543	07/11/1997
	US-6,346,803	02/12/2002	Grossnickle, Vaughn J., et al.	323	315	11/30/2000
	US-6,445,170	09/03/2002	Pangal, Amaresh , et al.	323	315	10/24/2000

**FOREIGN PATENT DOCUMENTS**

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T <sup>2</sup>
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**OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		LEE, CHEOL-HEE , et al., "A Temperature and Supply Insensitive CMOS Current", <u>EEE ICVC</u> , Available at <a href="http://asic.postech.ac.kr/2.Research/2.Publications/iconfer/08.pdf">http://asic.postech.ac.kr/2.Research/2.Publications/iconfer/08.pdf</a> , (October 1997), 498-500	
		LEE, SEUNG-HOON , "A Temperature and Supply-Voltage Insensitive CMOS Current Reference", <u>IEICE Trans. Electron</u> , Vol. E82-C, (Aug. 1999), pp. 1562-1566	
		LEE, C.-H. , et al., "All-CMOS Temperature Independent Current Reference", <u>Electronics Letters</u> , Vol. 32, No. 14, (July 4, 1996), pp. 1280-1281	
		NARENDRA, S , et al., "Sub-1 V Process-Compensated MOS Current Generation Without Voltage Reference", <u>IEEE Symposium on VLSI Circuits Digest of Technology Papers</u> , (2001), pp. 143-144	

**EXAMINER****DATE CONSIDERED**

Substitute Disclosure Statement Form (PTO-1449)

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. <sup>1</sup> Applicant's unique citation designation number (optional) <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached